TFE4188 - Introduction to Lecture 2

ICs and ESD

Goal

Understand the **real-world** constraints on our IC

Understand why you must **always handle ESD** on an IC

RPLY

The project for 2023 is to design an integrated temperature sensor. The hope is that some will tapeout on the Google/Efabless Open MPW shuttle

The **real world** constrains our IC

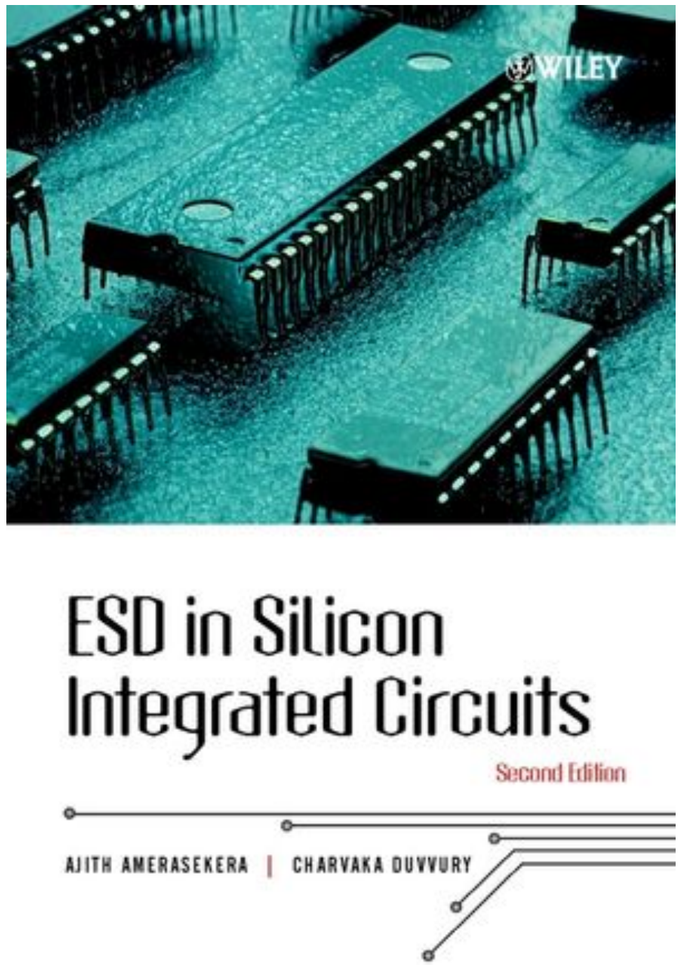
Q: What blocks must our IC include?

ESD

Electrostatic Discharge

If you make an IC, you must consider Electrostatic Discharge (ESD) Protection circuits

Standards for testing at JEDEC



When do ESD events occur?

Before/during PCB

Human body model (HBM)

Charged device model (CDM)

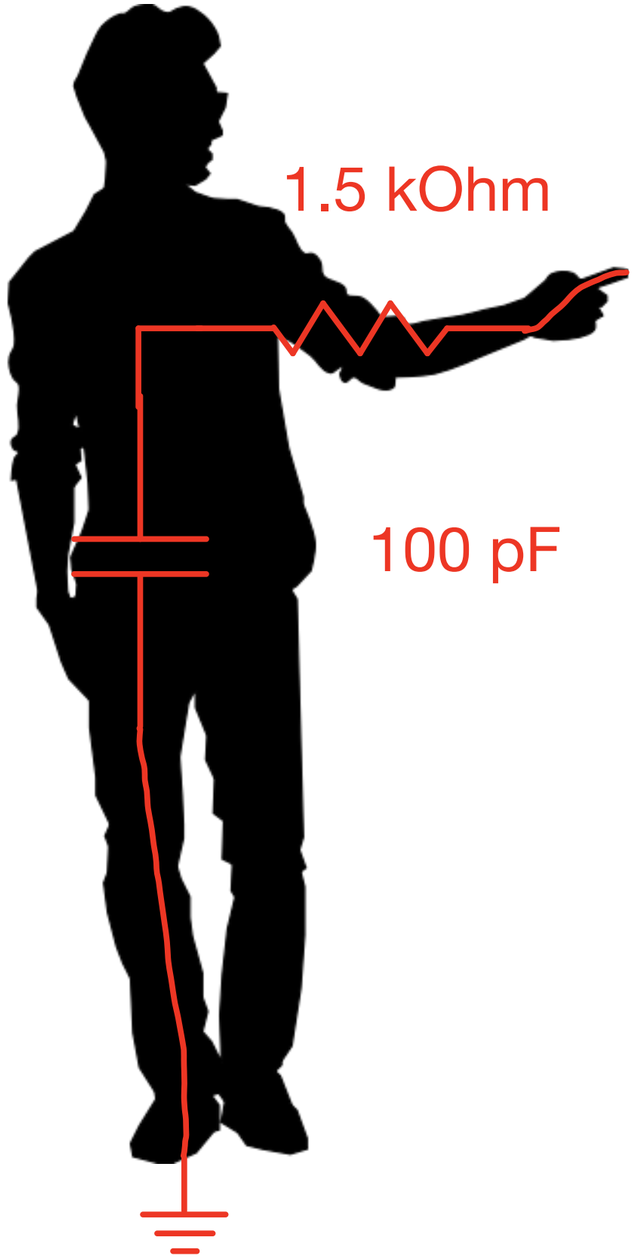
After PCB

Human body model (HBM)

System level ESD

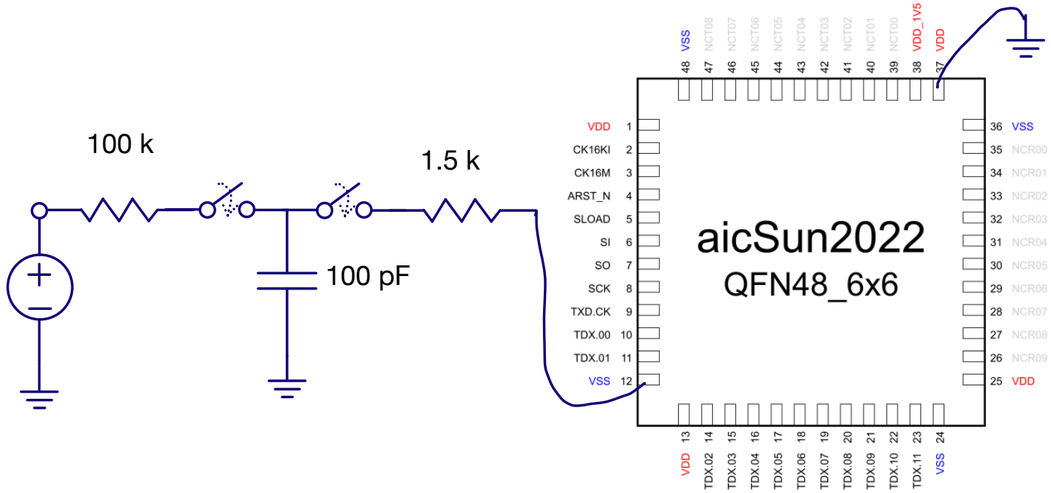
Human body model (HBM)

- Models a person touching a device with a finger
- **Long** duration (around 100 ns)
- Acts like a current source into a pin
- Can usually be handled in the I/O ring
- 4 kV HBM ESD is 2.67 A peak current



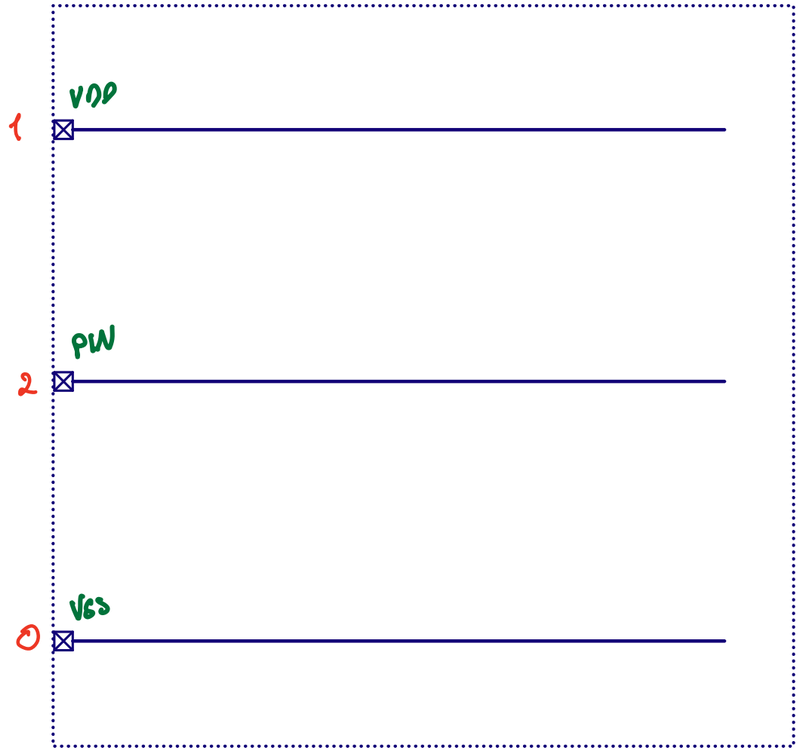
An ESD zap example

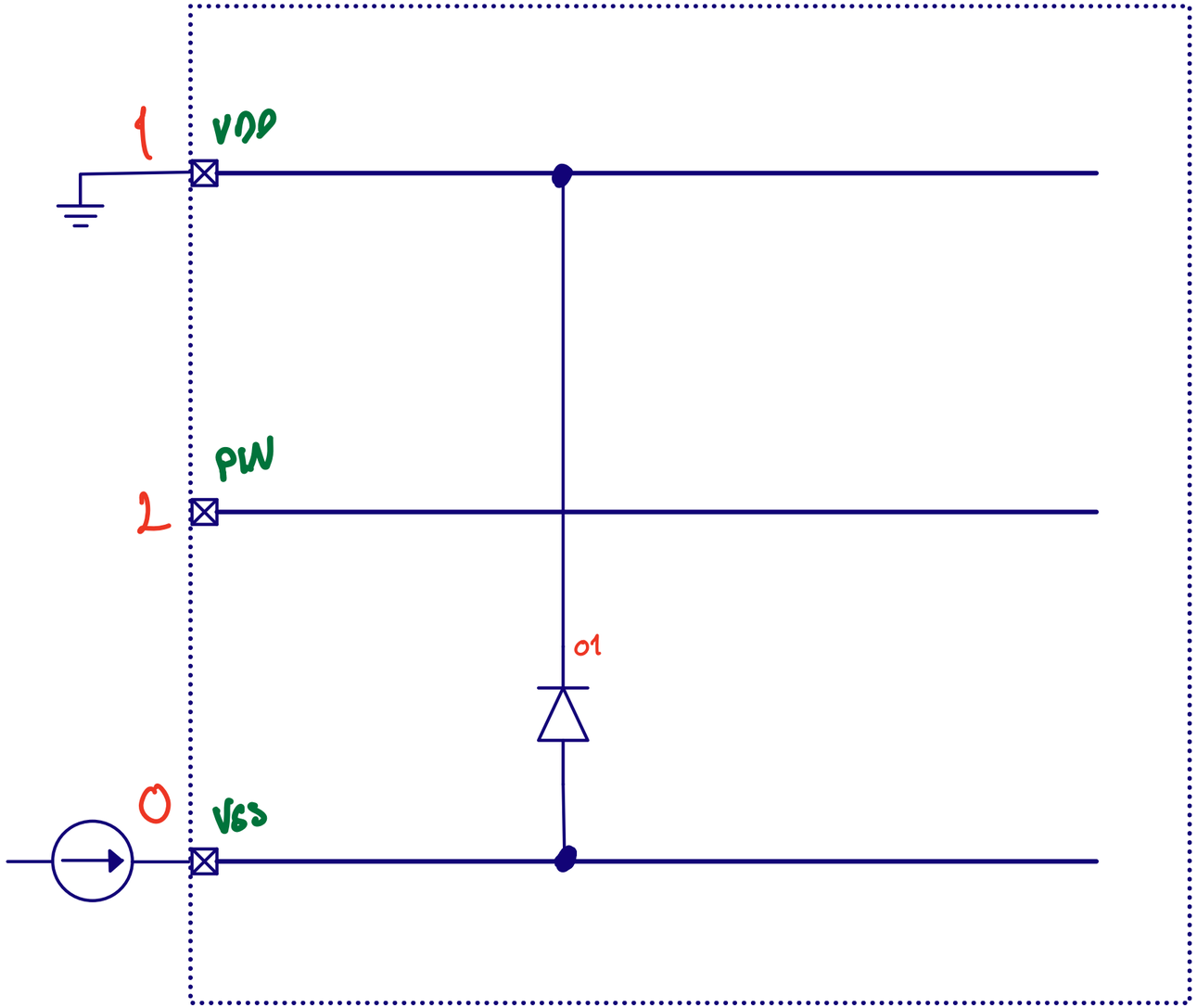
Imagine a ESD zap between VSS and VDD. How can we protect the device?

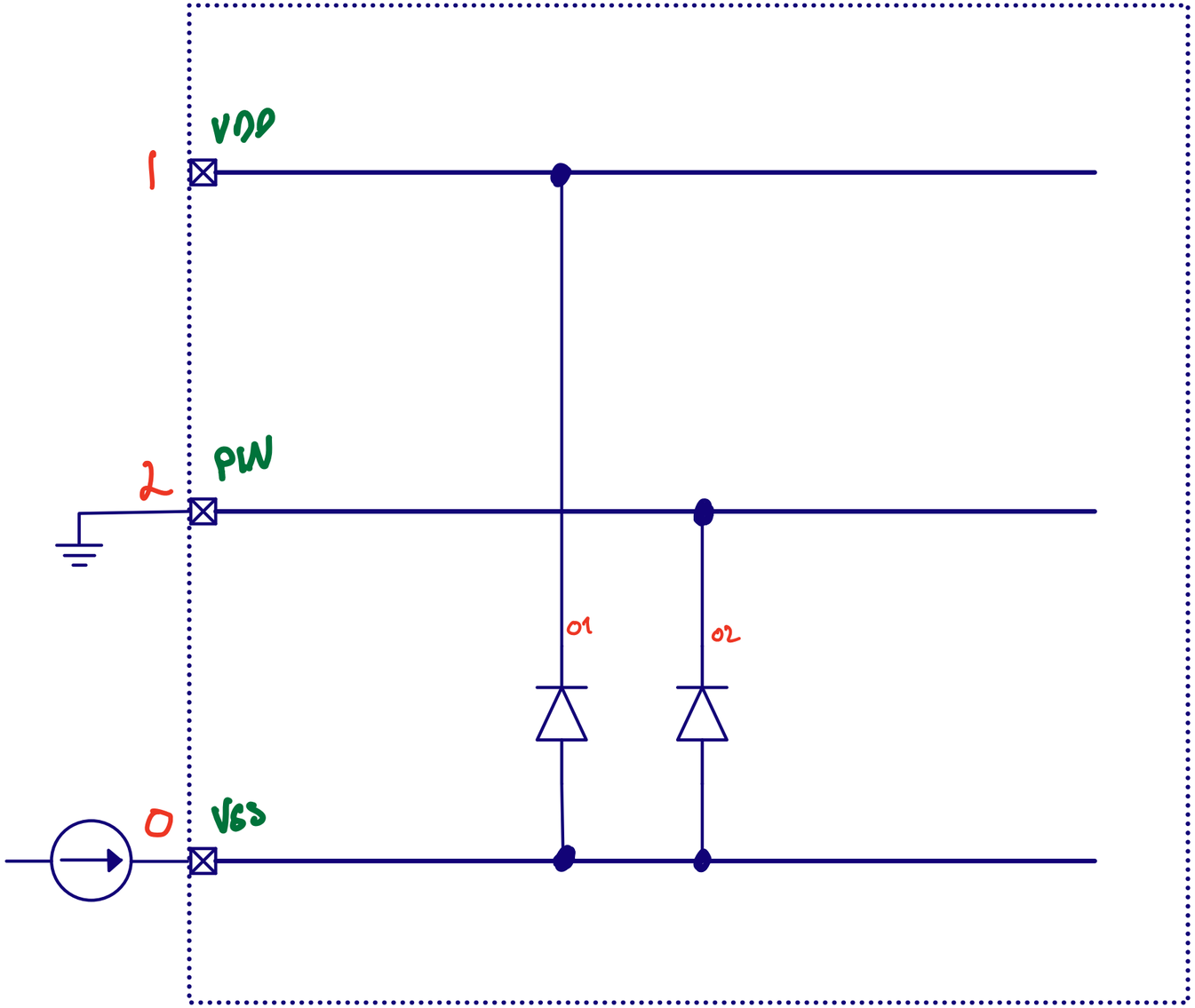


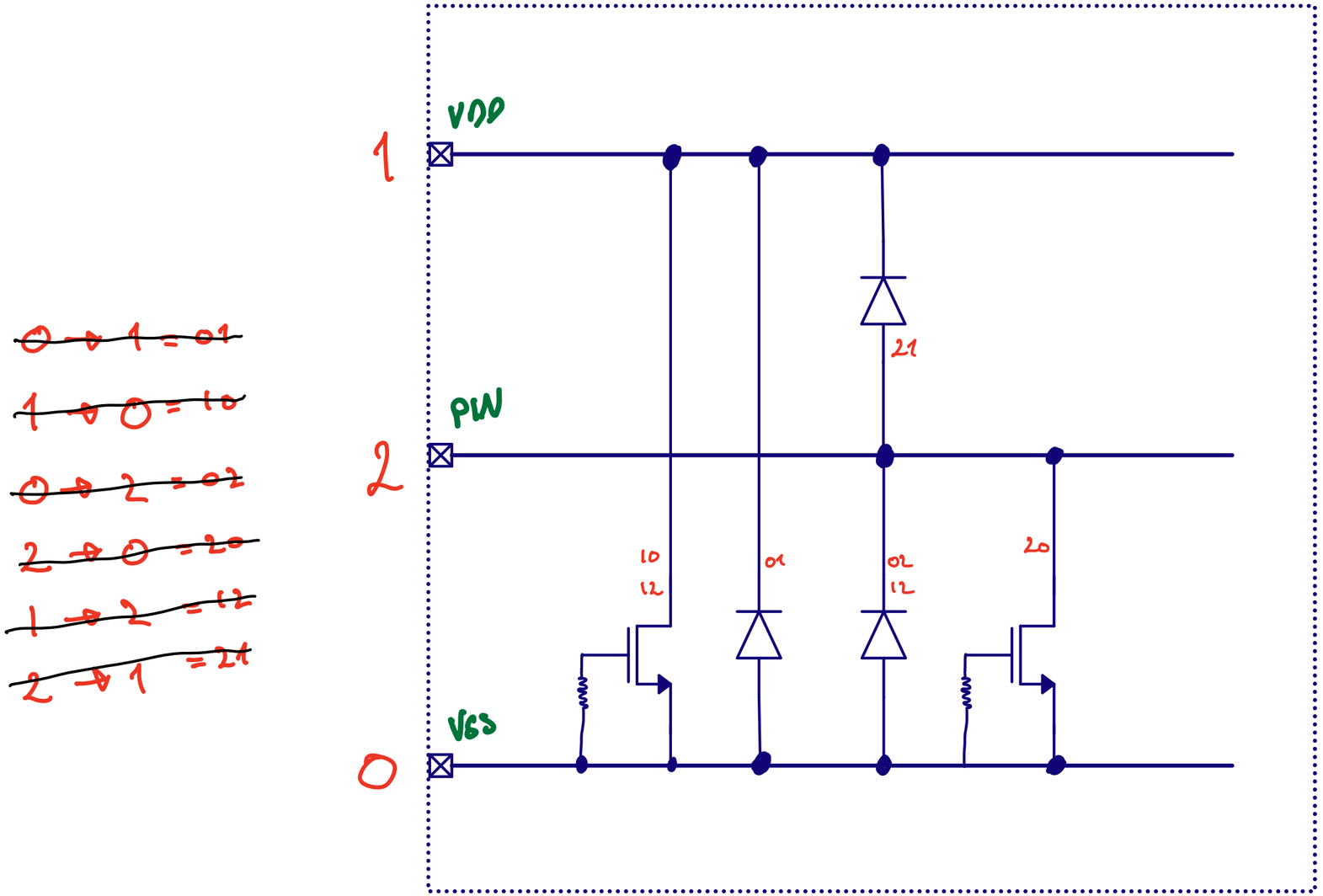
Permutations

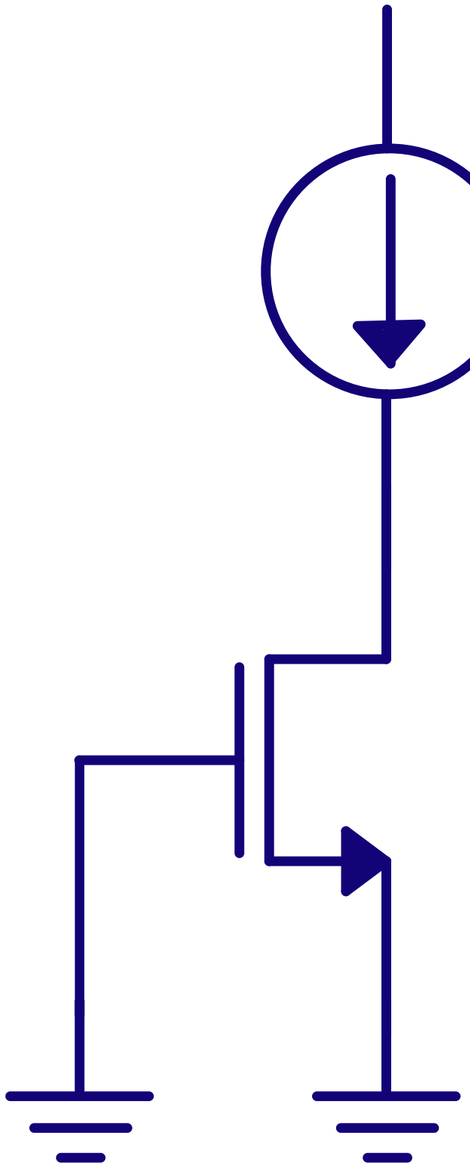
0 → 1 VSS → VDD
1 → 0 VDD → VSS
0 → 2 VSS → PIN
2 → 0 PIN → VSS
1 → 2 VDD → PIN
2 → 1 PIN → VDD




1
VDD
PW
2
D1
0
VSS


VDD
1
PW
2
D1
D2
0
VSS


0 → 1 = 01
1 → 0 = 10
0 → 2 = 02
2 → 0 = 20
1 → 2 = 12
2 → 1 = 21
1
VDD
2
PW
0
VSS
21
10
12
01
02
12
20



2,6A

Q: Why does this work?

If you don't do the layout right[3]

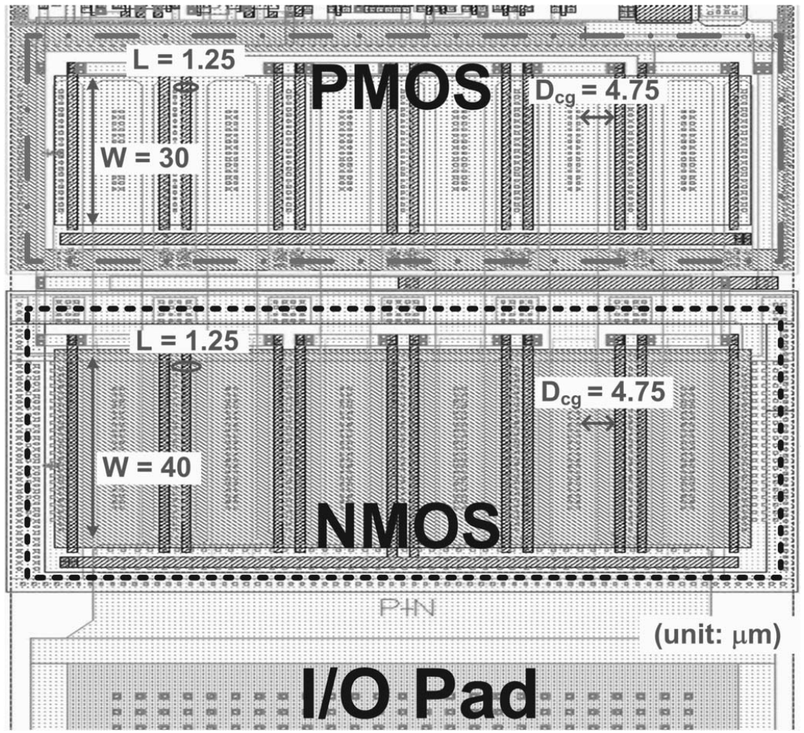


Fig. 5. Layout top view of the self-protecting fully silicided I/O buffer in a CMOS IC product.

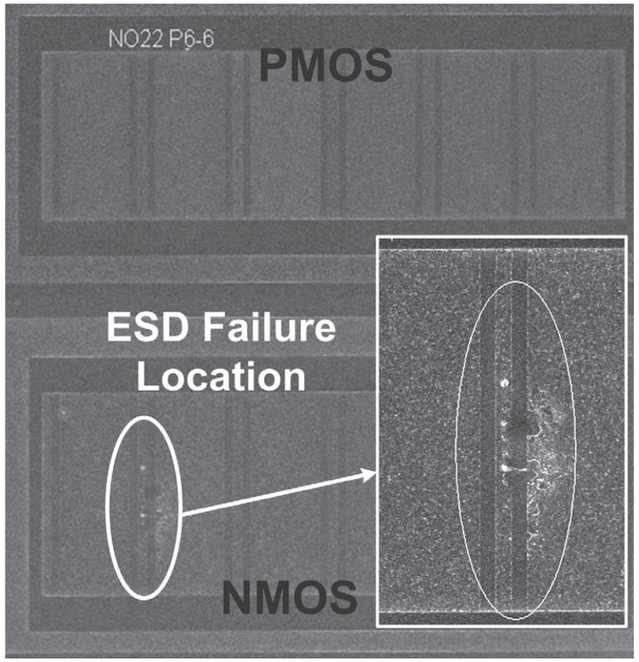
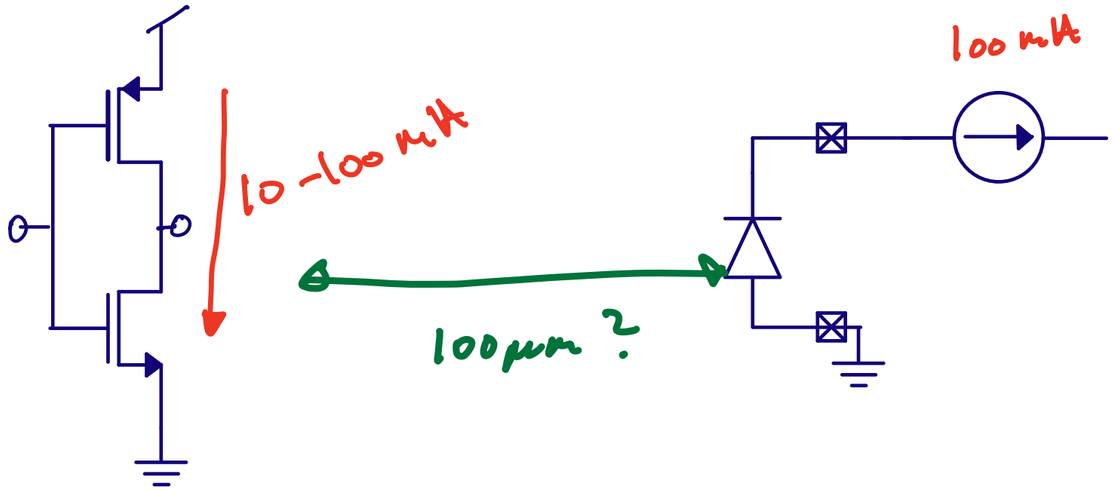


Fig. 6. SEM image of the fully silicided I/O buffer without ballasting after 2-kV PS-mode ESD stress. ESD failure is found on only one finger of the driver NMOS. Current filamentation is also observed on the surface of the driver NMOS without ballasting.

[3] New Ballasting Layout Schemes to Improve ESD Robustness of I/O Buffers in Fully Silicided CMOS Process



Q: How can current in one place lead to a current somewhere else?

You must **always handle ESD** on an IC

- Do everything yourself
- Use libraries from foundry
- Get help www.sofics.com

Thanks!