date: 2024-03-01

TFE4188 - Lecture 7

Voltage regulation

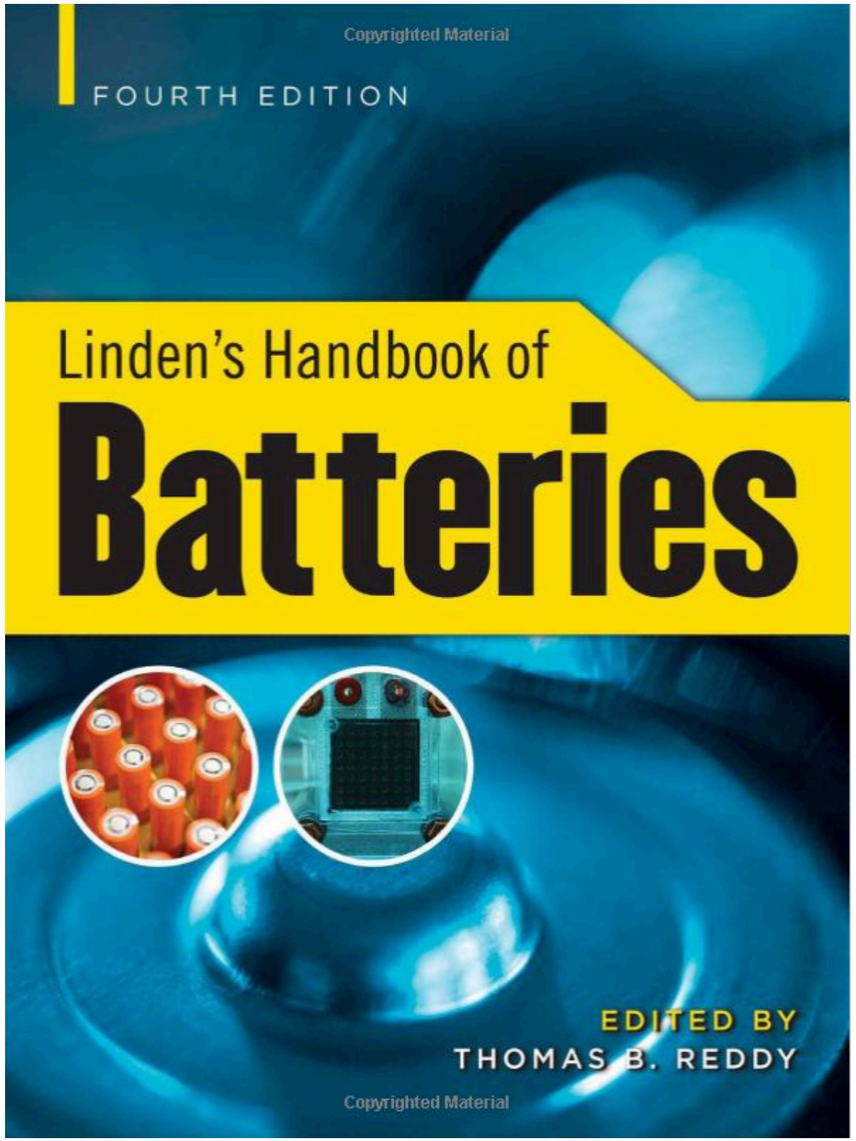
Goal

Why do we need voltage regulation

Introduction to **linear regulators**

Introduction to **switched regulators**

Why



Voltage source

	Chemistry	**Voltage [V]**
Primary Cell	LiFeS2 , Zn/ Alk/MnO2 , LiMnO2	0.8 - 3.6
Secondary Cell	Li-Ion	2.5 - 4.3
USB	-	4.0 - 6.5 (20)

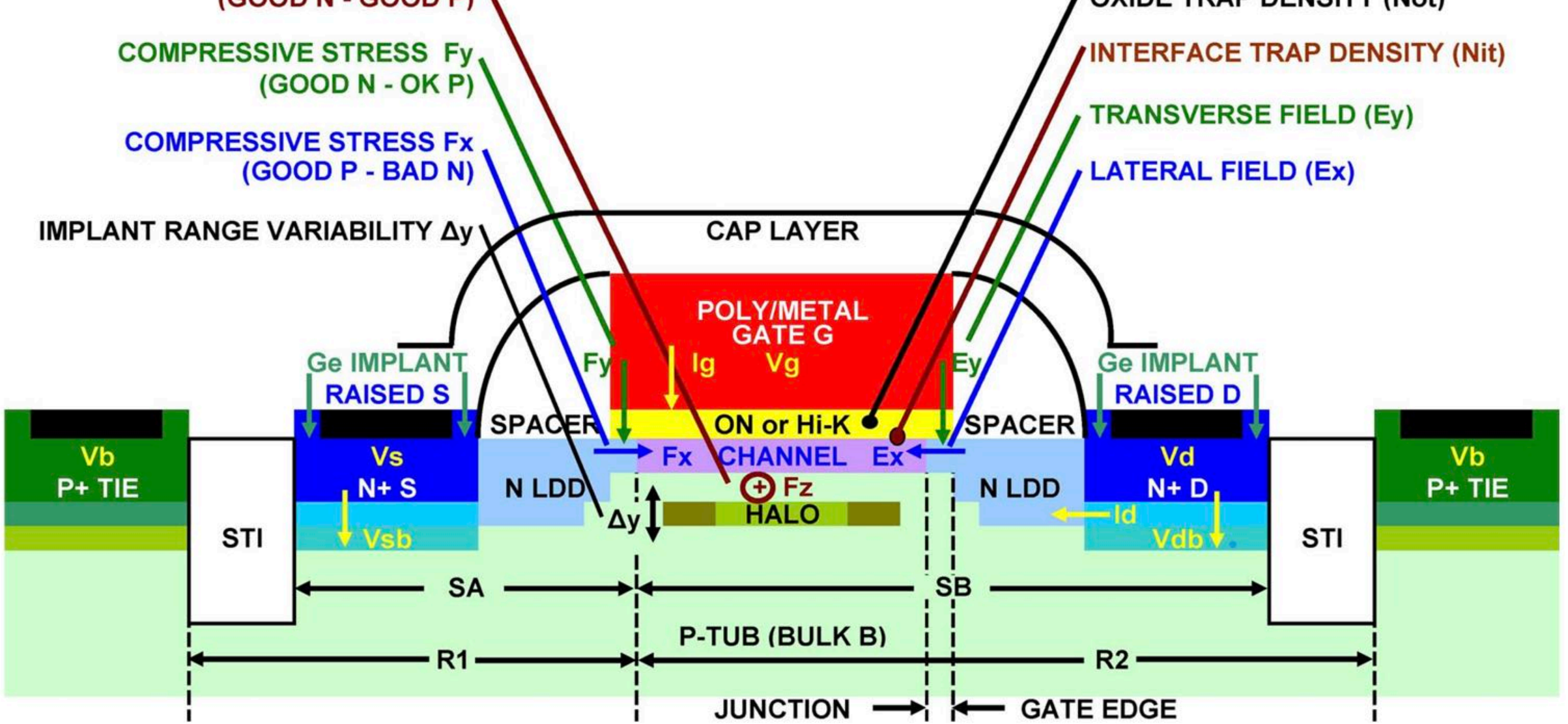
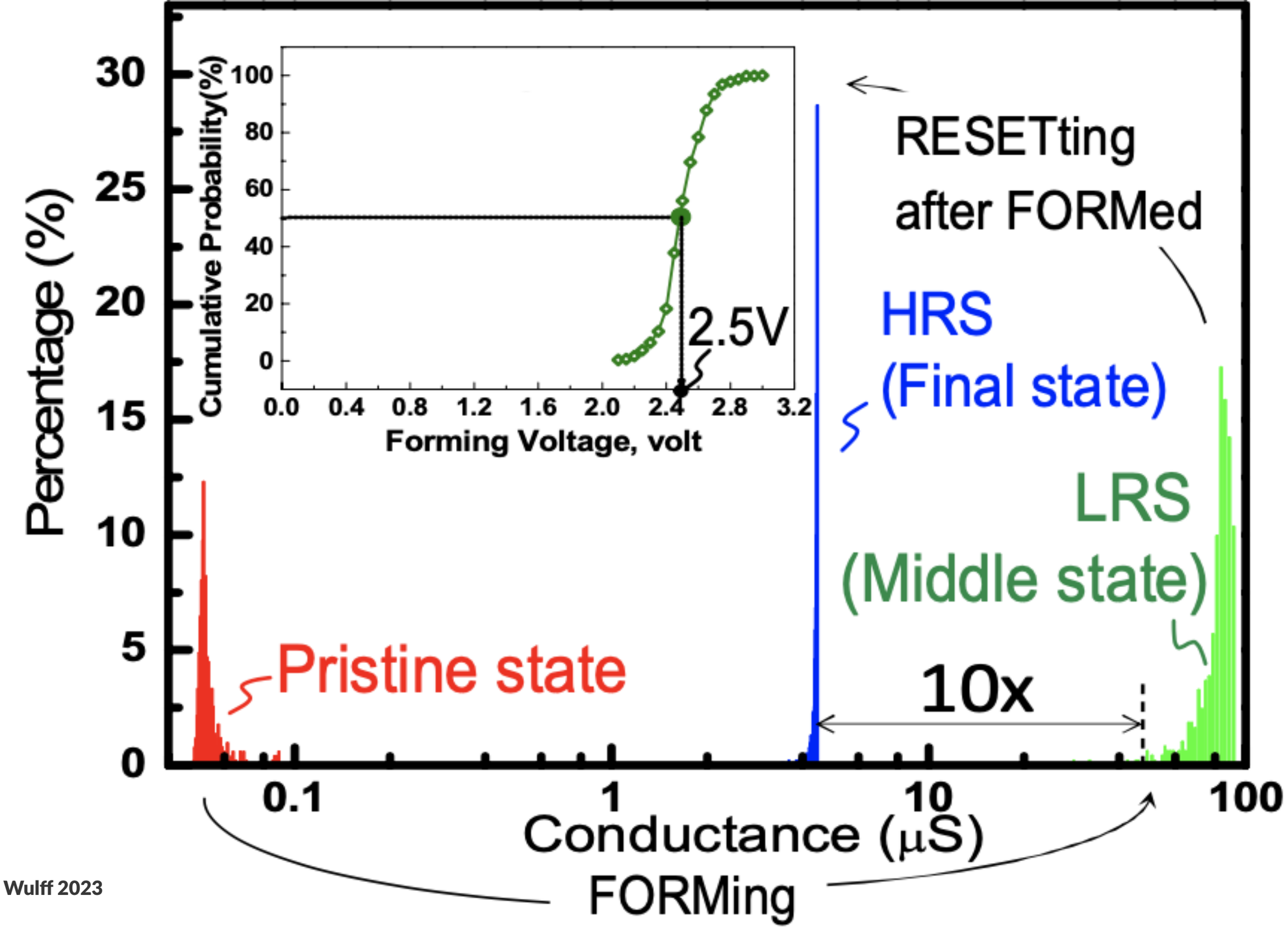


Fig. 2. ***NMOS cross-section. In addition to stress from cap layers and Ge raised source-drain (S-D) implants, device dimensions such as distance from source-channel boundary to nearby STI (SA and SB), proximity and regularity of overlying metal patterns, and short distances to other device patterns within the local*** $(< 2\ \mu m)$ ***stress field induce transverse*** (F_y) ***and lateral (*** F_x ***and*** F_z***) stress components, which affect threshold and mobility. Increasing the distance to P+ ties increases local tub (bulk) resistance components R1 and R2, which isolate the device MOS model substrate node from the device subcircuit symbol*** V_b ***node and degrade HF performance. Hot carrier reliability stress is dependent on the sum of***

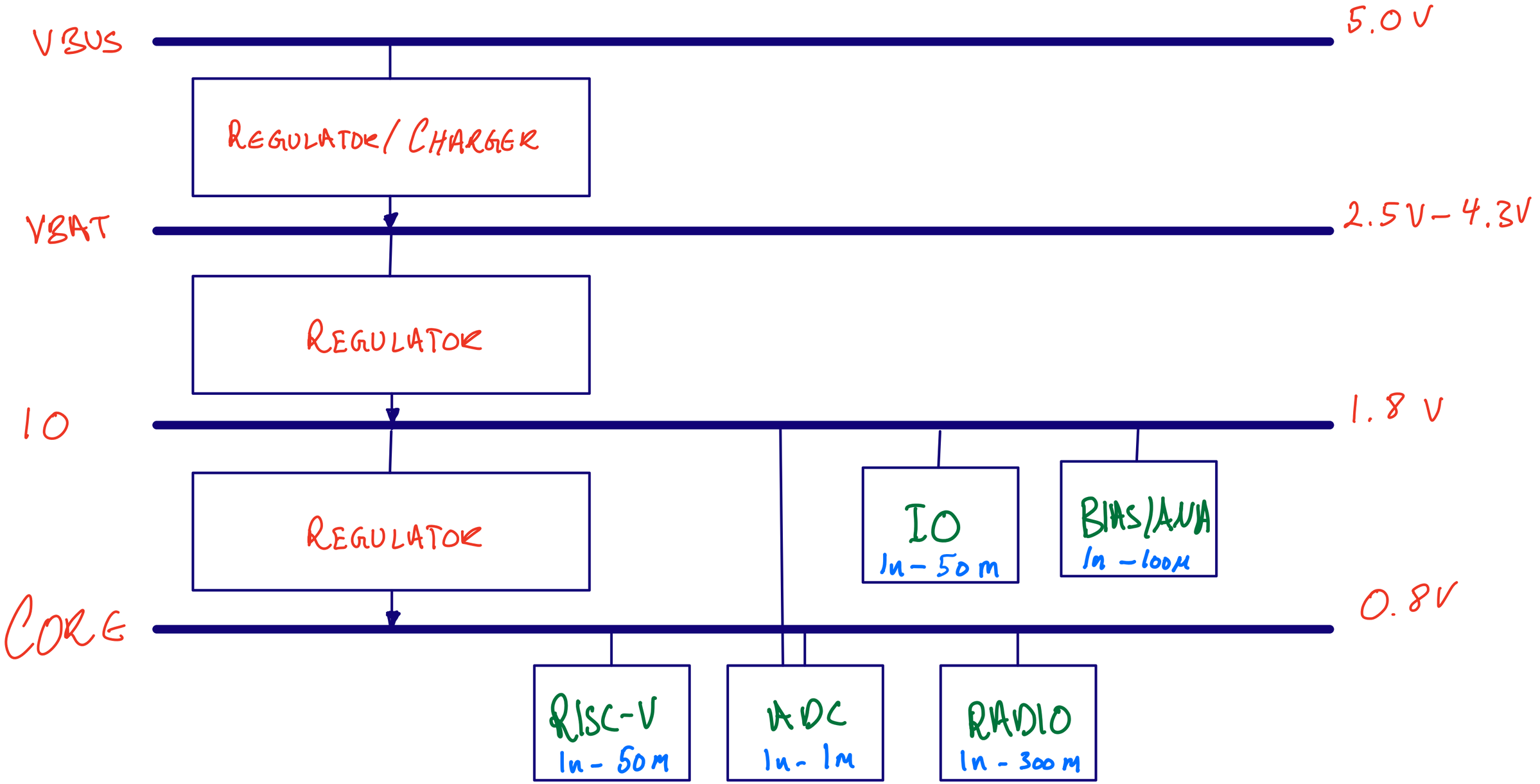

Percentage (%)
30
25
20
15
10
5
0
0.1
1
10
100
Conductance (μS)
FORMing
Pristine state
HRS
(Final state)
LRS
(Middle state)
10x
RESETting
after FORMed
Cumulative Probability(%)
100
80
60
40
20
0
0.0
0.4
0.8
1.2
1.6
2.0
2.4
2.8
3.2
Forming Voltage, volt
2.5V

Core voltage

Node [nm]	Voltage [V]
180	1.8
130	1.5
55	1.2
22	0.8

IO voltage

Voltage [V]
5.0
3.0
1.8
1.2


VBUS
5.0 V
REGULATOR / CHARGER
VBAT
2.5V - 4.3V
REGULATOR
IO
1.8 V
REGULATOR
IO
In - 50 m
BIAS/ANA
In - 100µ
CORE
0.8V
RISC-V
In - 50 m
ADC
In - 1m
RADIO
In - 300 m

Name	Voltage	Min [nA]	Max [mA]	PWR DR [dB]
VDD_VBUS	5	10	500	77
VDD_VBAT	4	10	400	76
VDD_IO	1.8	10	50	67
VDD_CORE	0.8	10	350	75

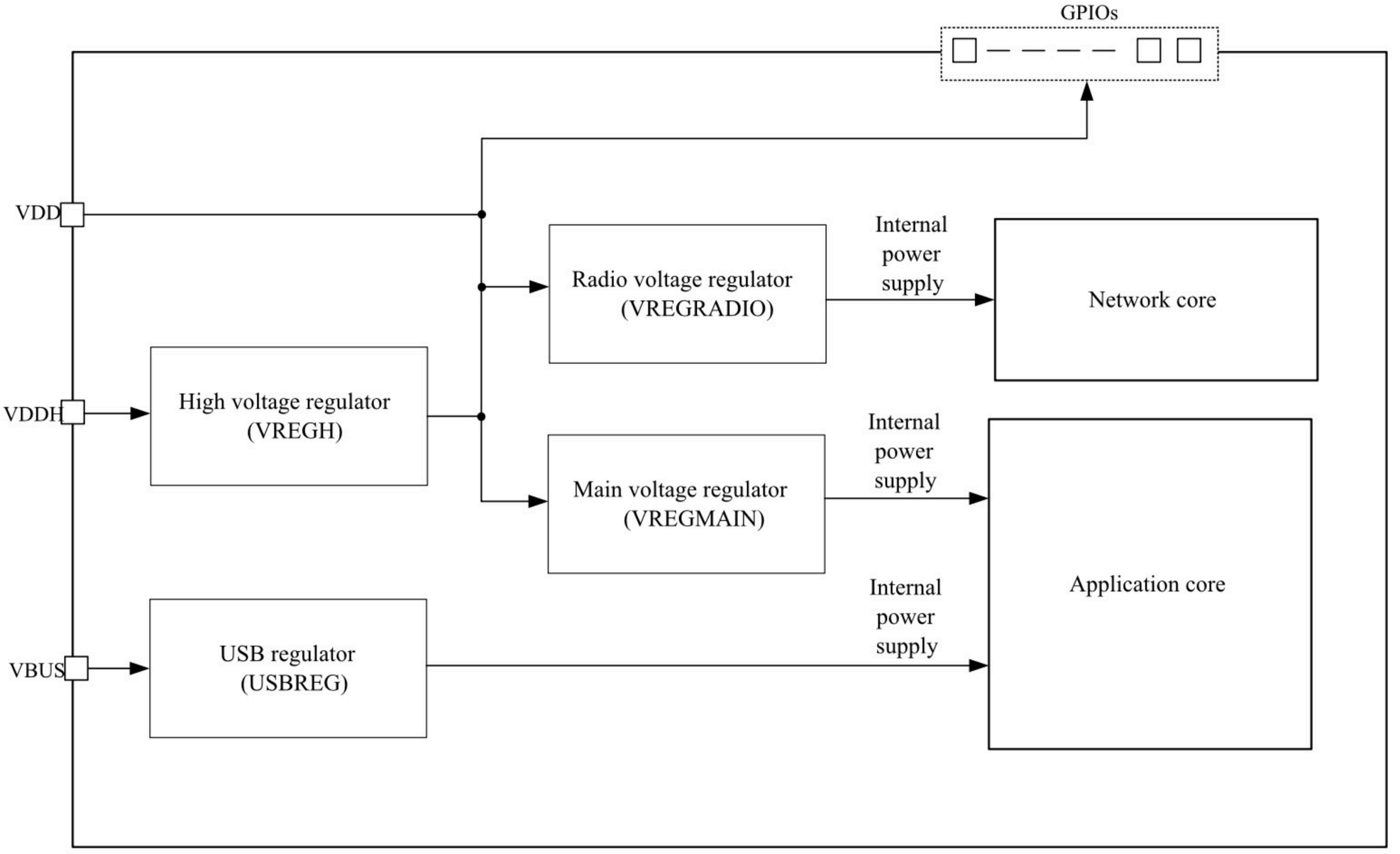
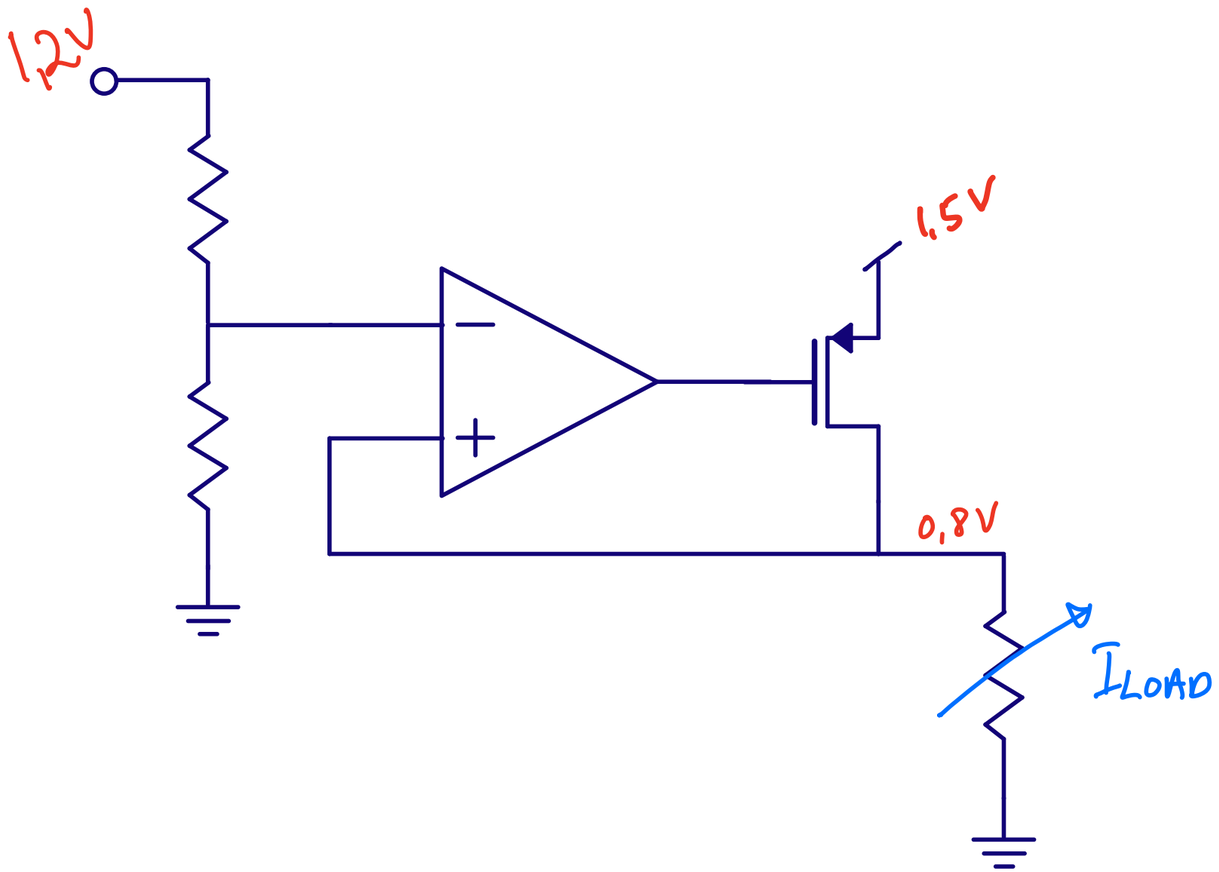


Figure 1. Regulators used in nRF5340

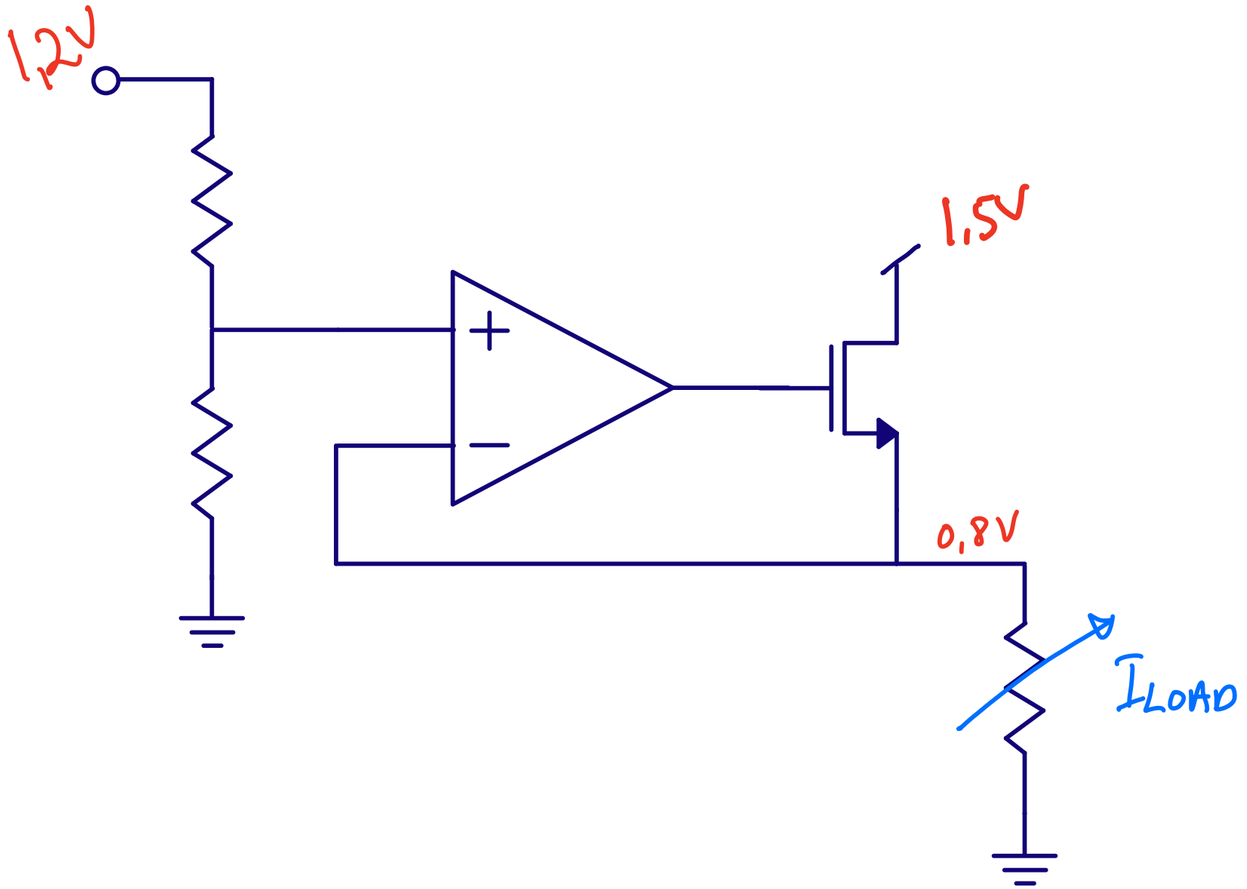
Linear Regulators



PMOS pass-fet

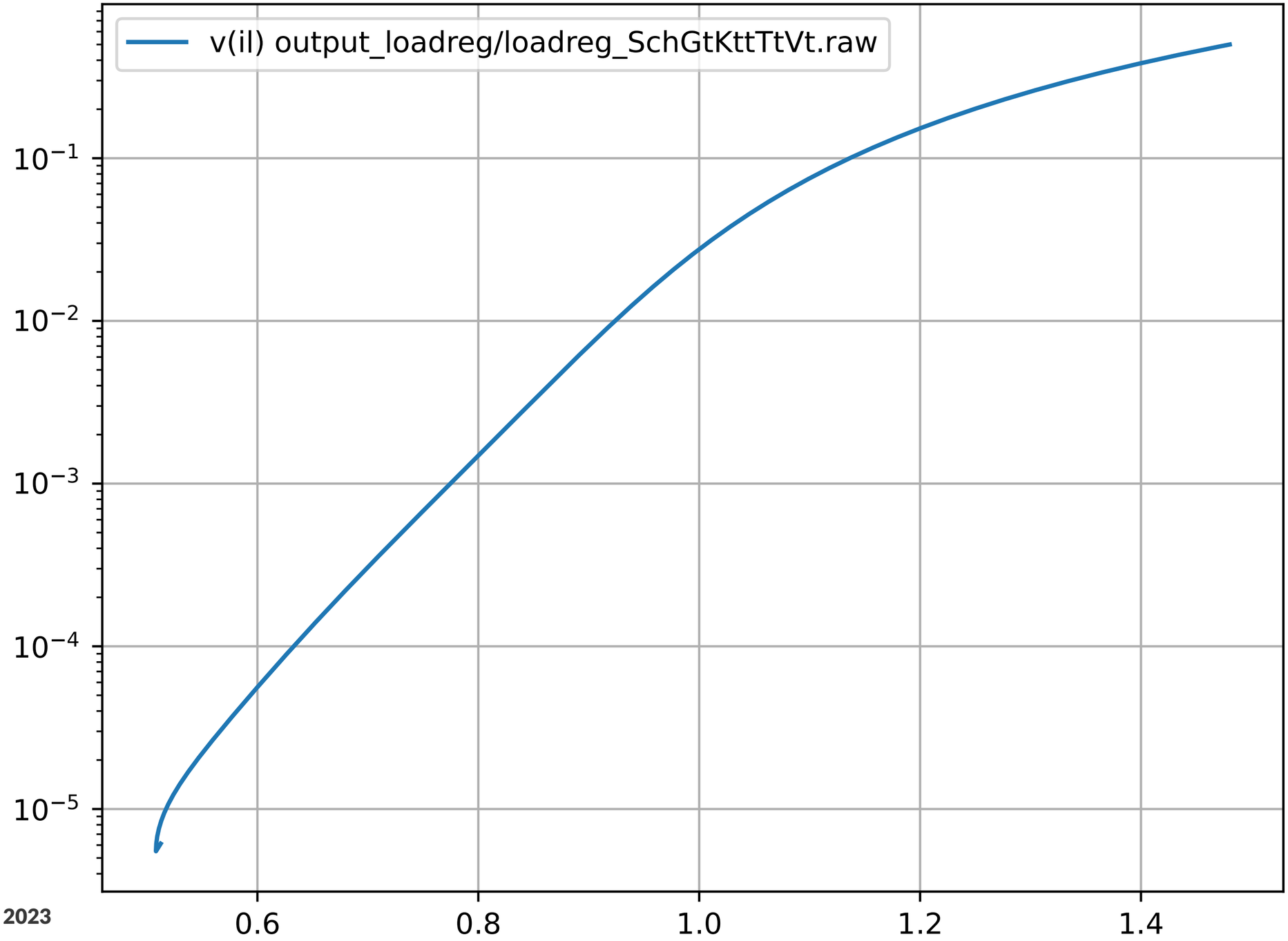
Parameter	Description	Unit
Load regulation	How much does the output voltage change with load current	V/A
Line regulation	How much does the output voltage change with input voltage	V/V
Power supply rejection ratio	What is the transfer function from input voltage to output voltage? The PSRR at DC is the line regulation	dB
Max current	How much current can be delivered through the pass-fet?	A
Quiescent current	What is the current used by the regulator	A
Settling time	How fast does the output voltage settle at a current step	s

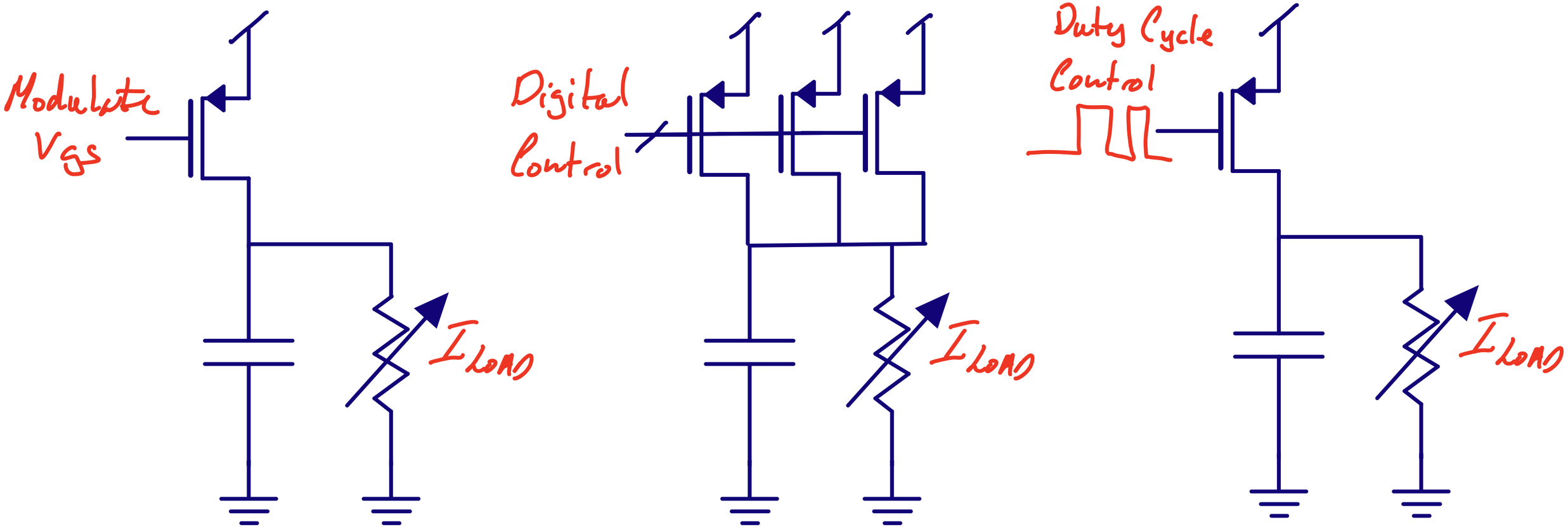
NMOS pass-fet



Testbench for LDO pass-fet

```
* Pass-fet
XM1 OUT G VDD VDD sky130_fd_pr__pfet_01v8 L=0.252 W=11.52 nf=2 ...  m=1000

* Reference
VREF VREF 0 dc 0.8

* OTA
BOTA G 0 V=(1 + tanh(-1000*(v(vref) -v(out) )))/2*{AVDD}

* Load cap
CL OUT 0 1u

* Current load
ILOAD OUT 0 pwl 0 0 1u 0 50u 0.5
```


v(il) output_loadreg/loadreg_SchGtKttTtVt.raw
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
0.6
0.8
1.0
1.2
1.4


Modulate
V_{GS}
I_{LOAD}
Digital
Control
I_{LOAD}
Duty Cycle
Control
I_{LOAD}

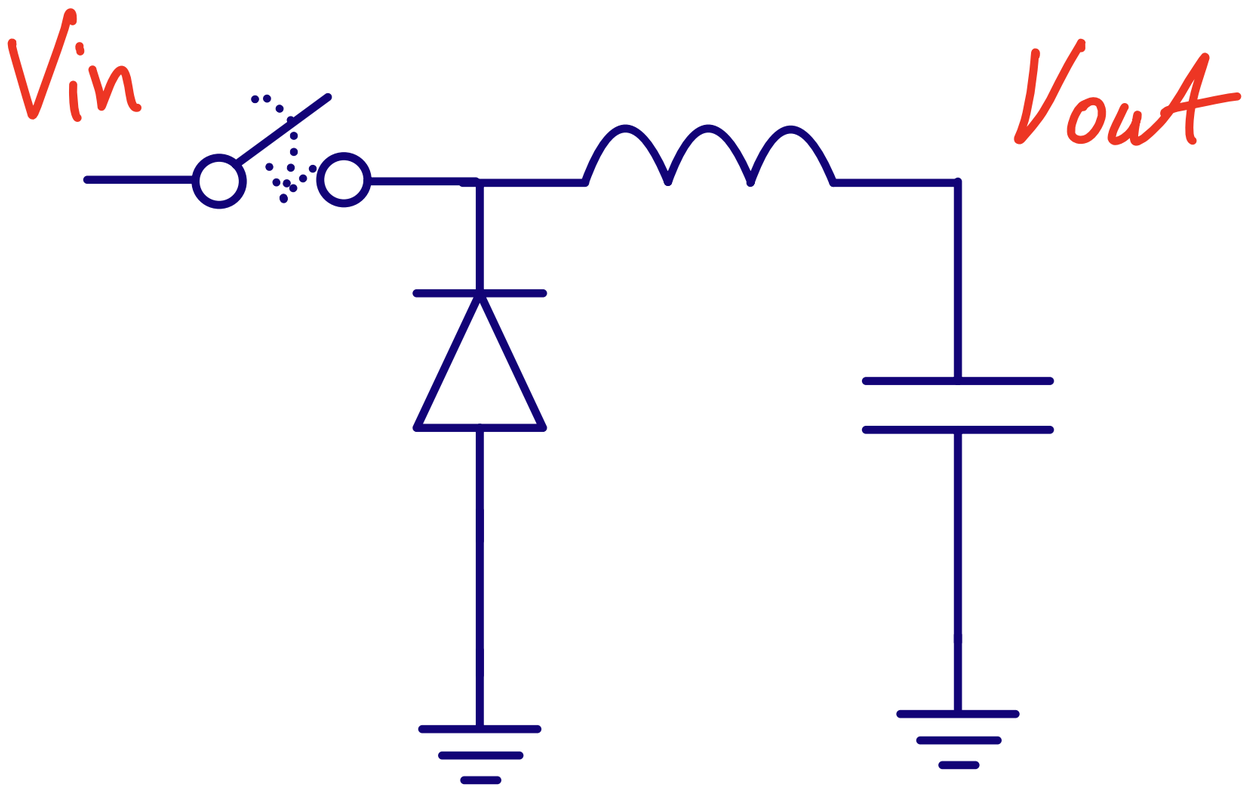
Switched Regulators

Principles of switched regulators

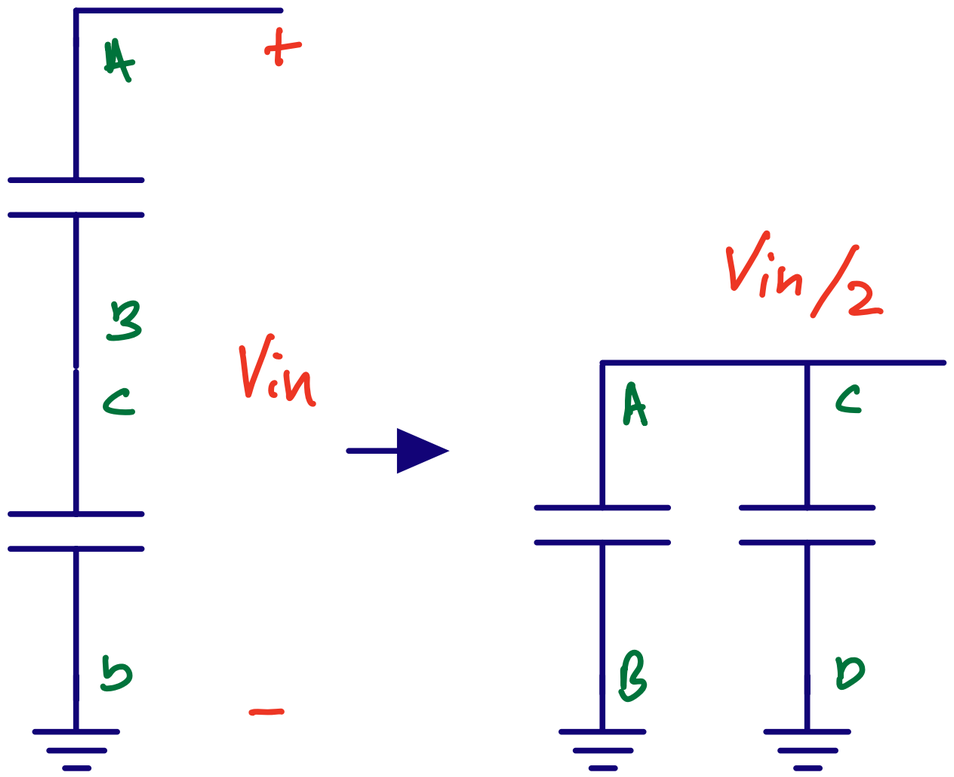
There is a big difference between the idea for a circuit, and the actual implementation. A real DC/DC implementation may seem overwhelming.

Just look at figure 7 in A 10-MHz 2–800-mA 0.5–1.5-V 90% Peak Efficiency Time-Based Buck Converter With Seamless Transition Between PWM/PFM Modes

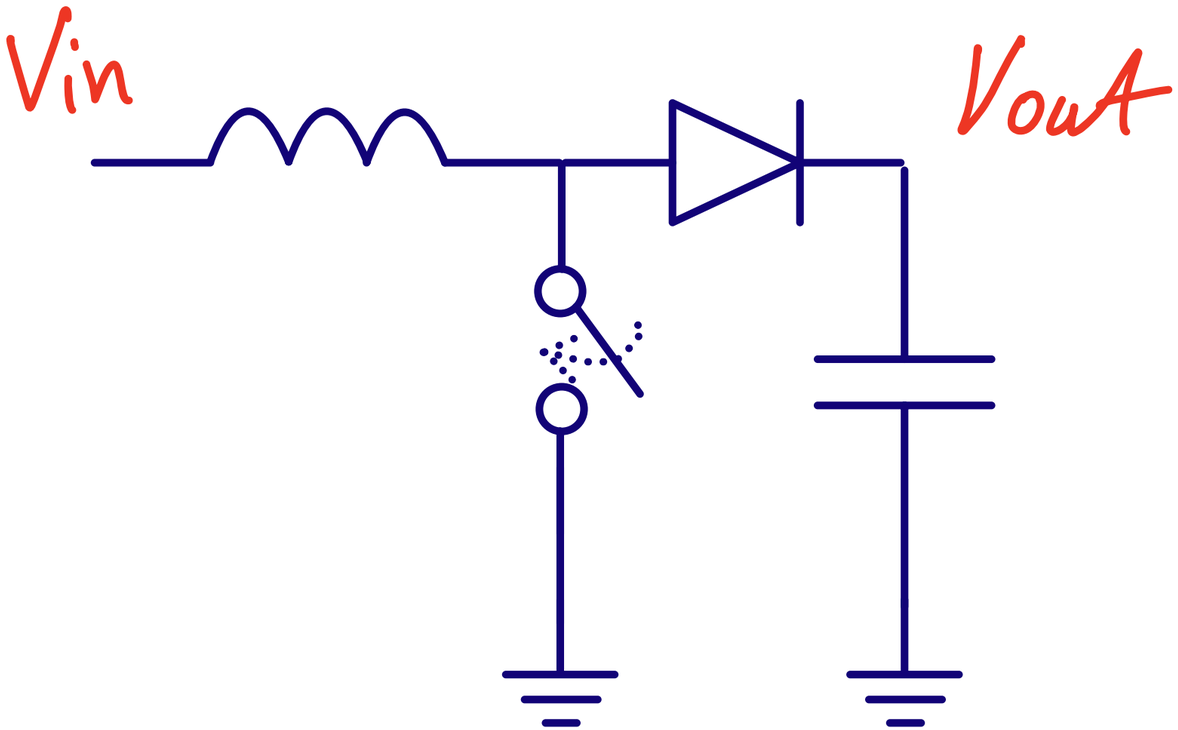
Inductive BUCK DC/DC



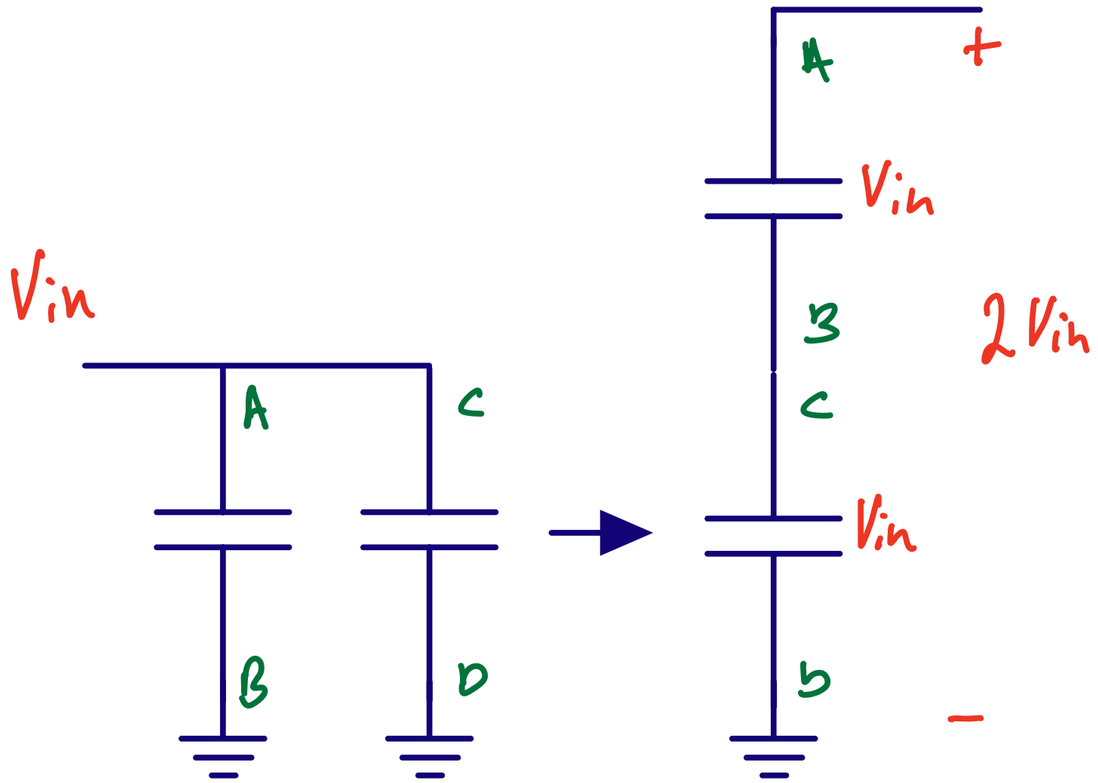
Capacitive BUCK DC/DC



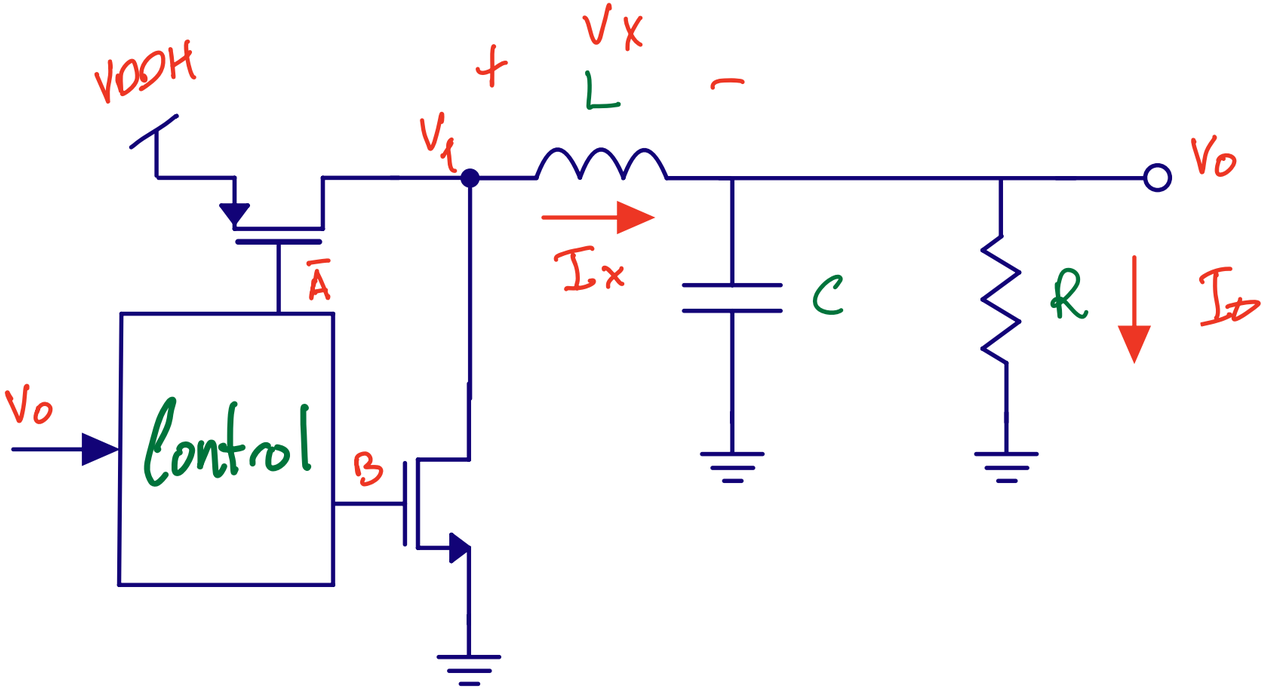
Inductive BOOST DC/DC



Capacitive BOOST DC/DC



Inductive DC/DC converter details

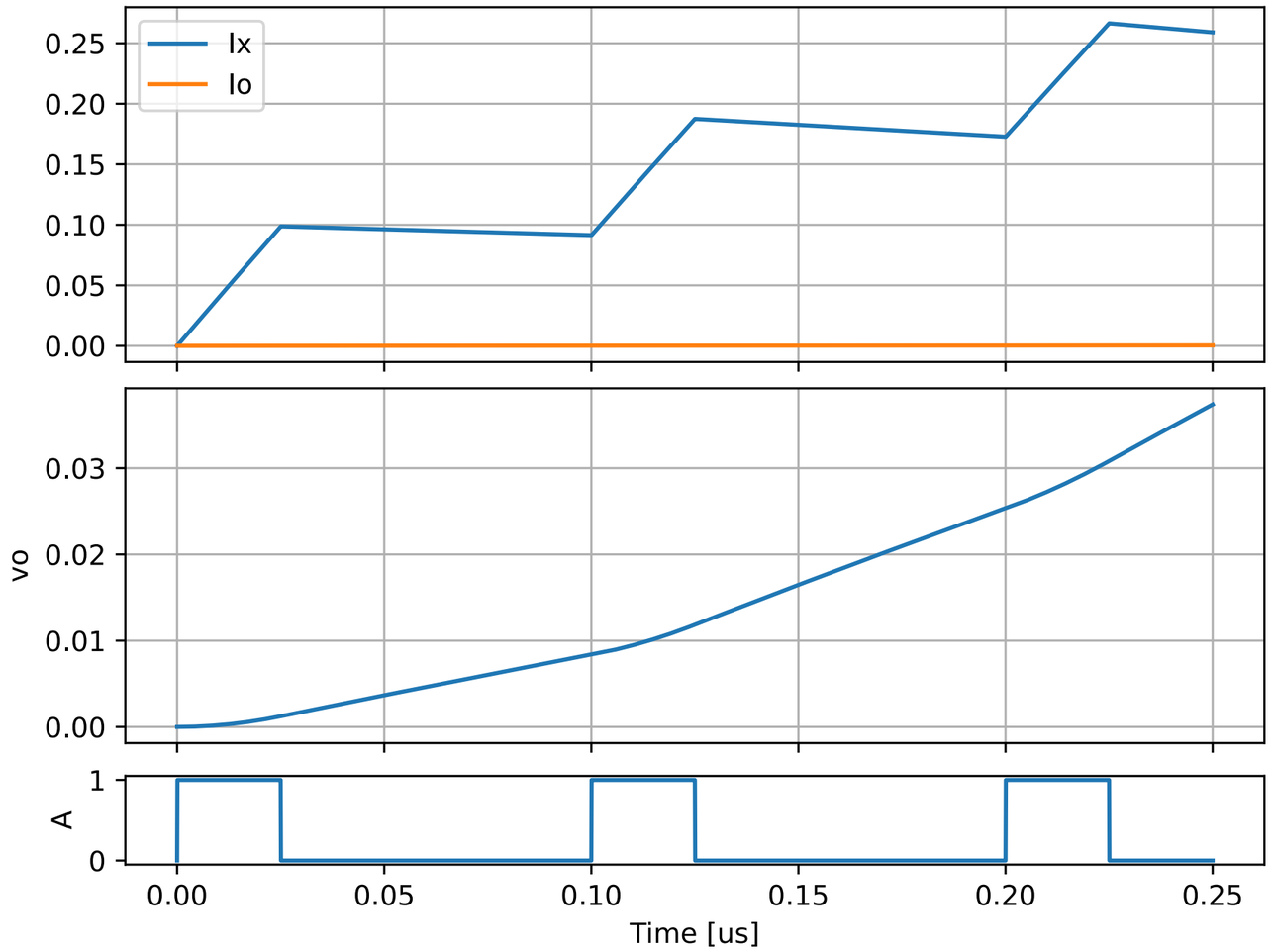


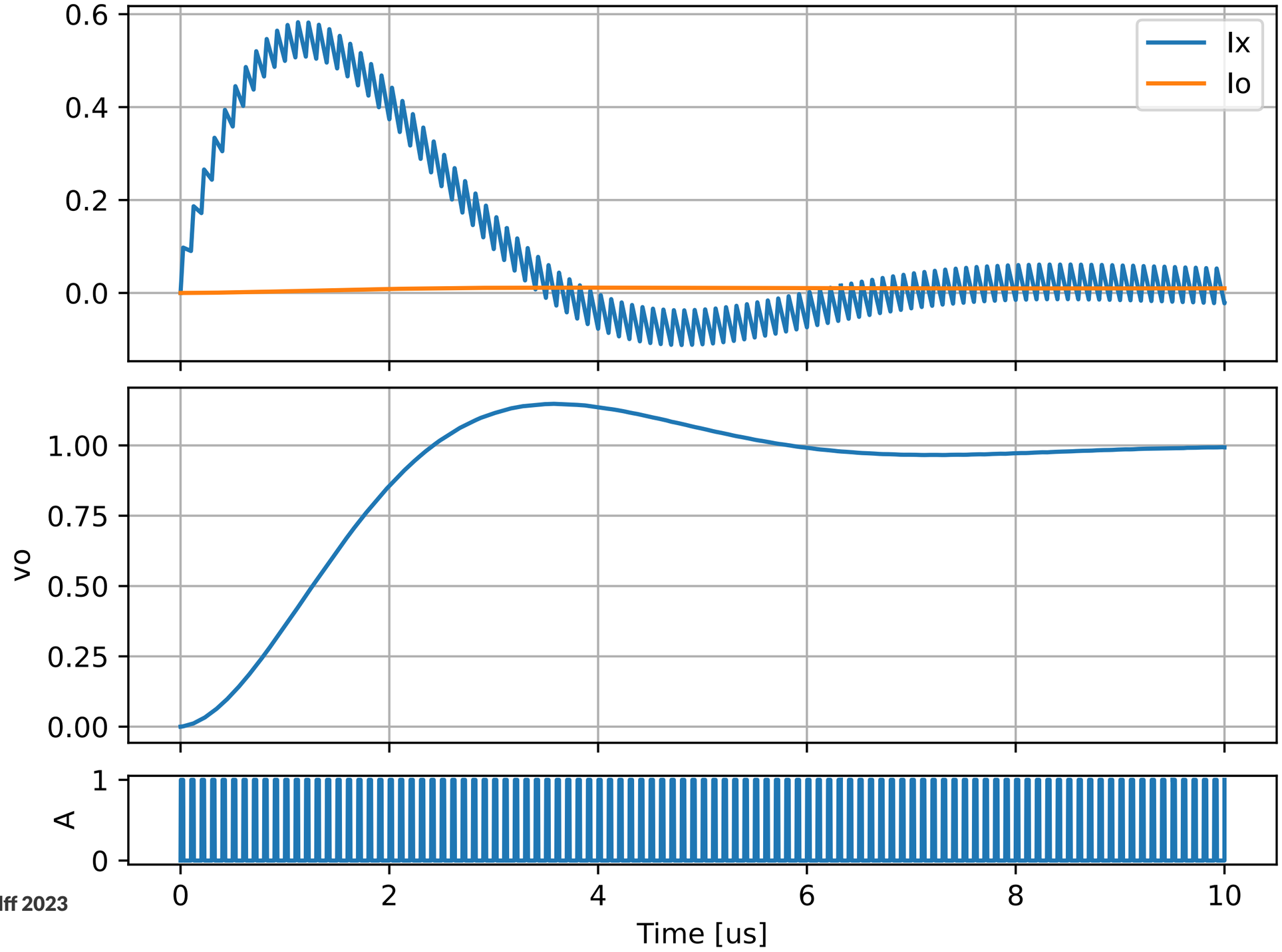
$$I_x(t) = \frac{1}{L}\int V_x(t)dt$$

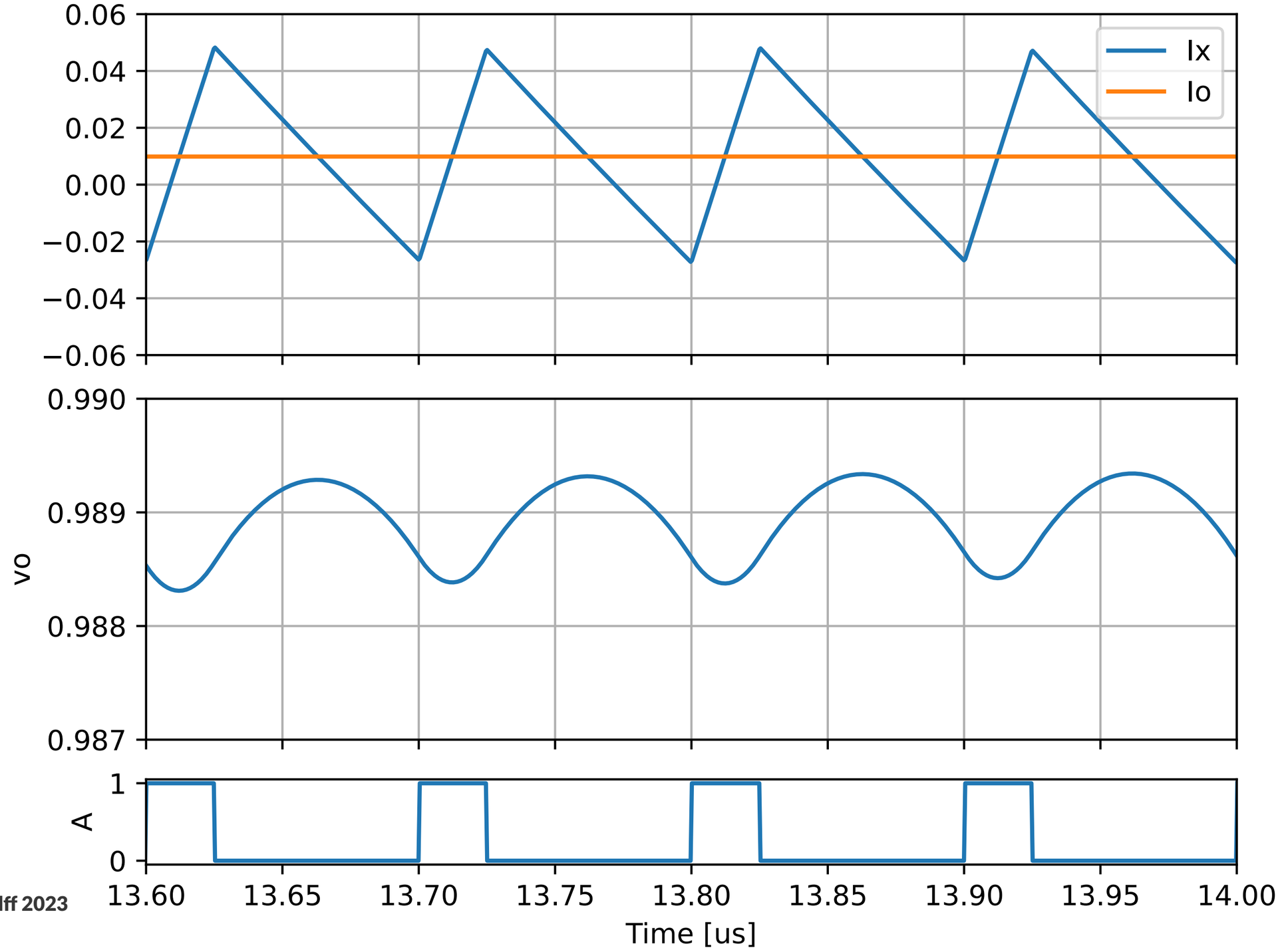
$$V_o(t) = \frac{1}{C}\int (I_x(t) - I_o(t))dt$$

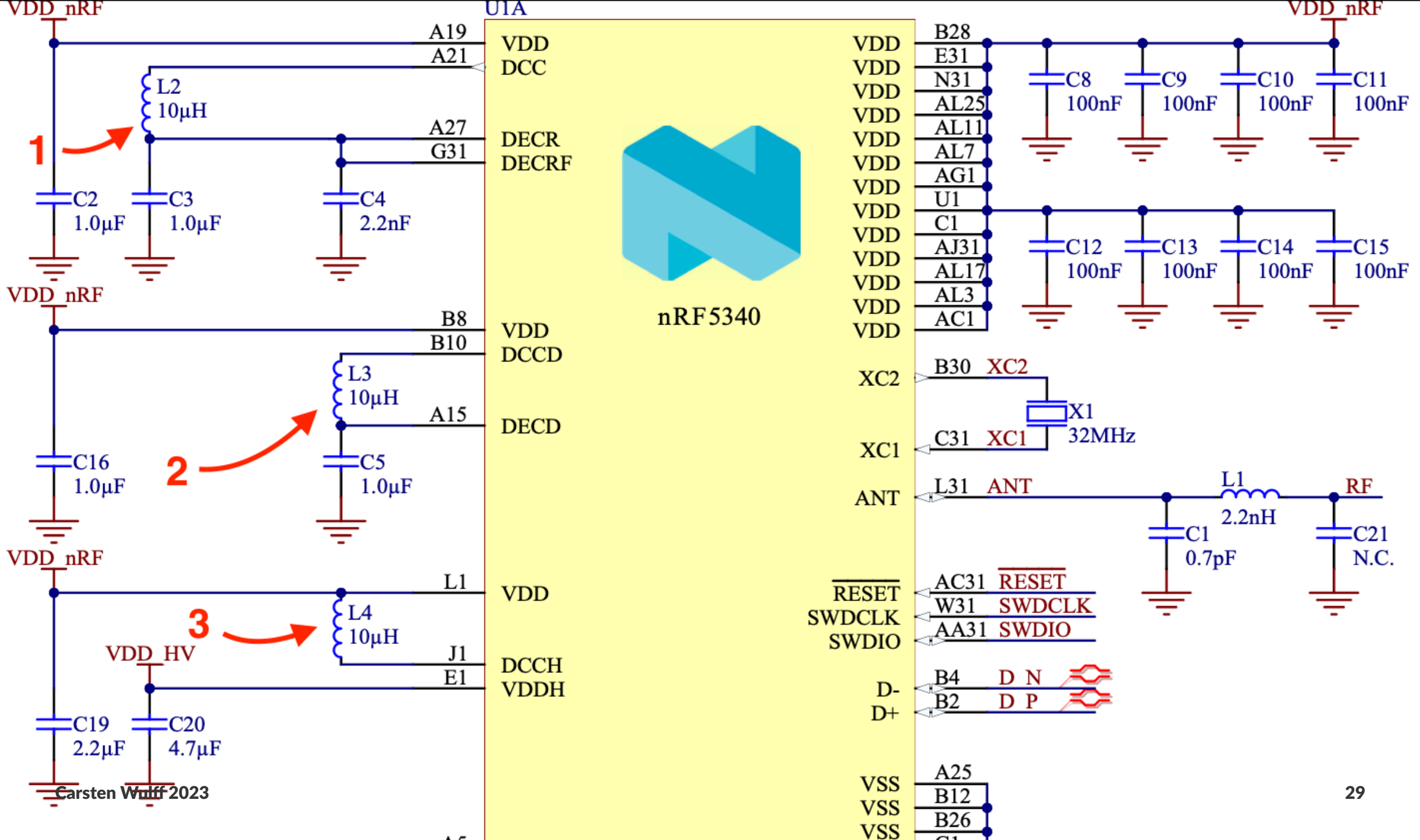
Pulse width modulation (PWM)

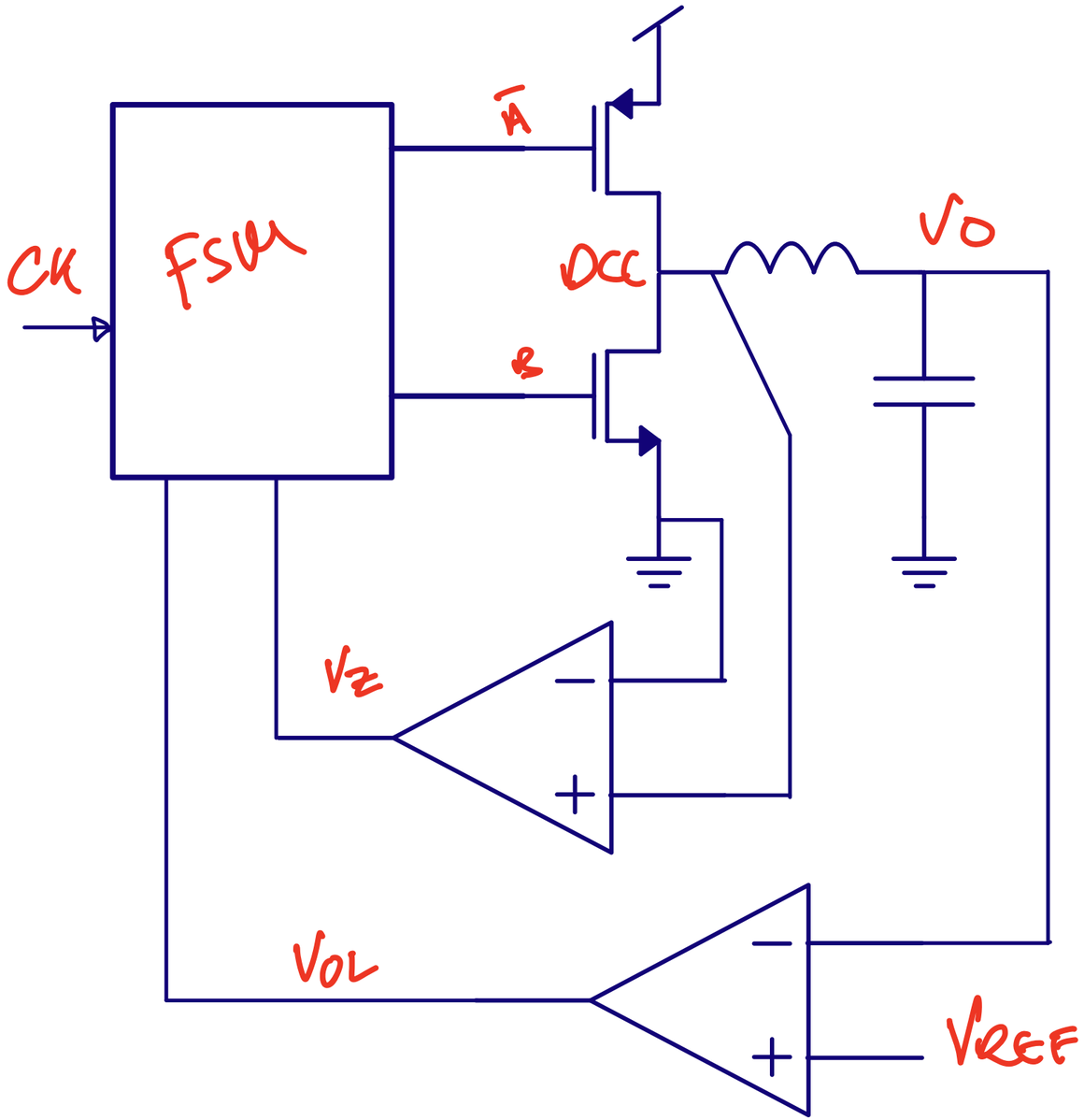
Jupyter PWM BUCK model



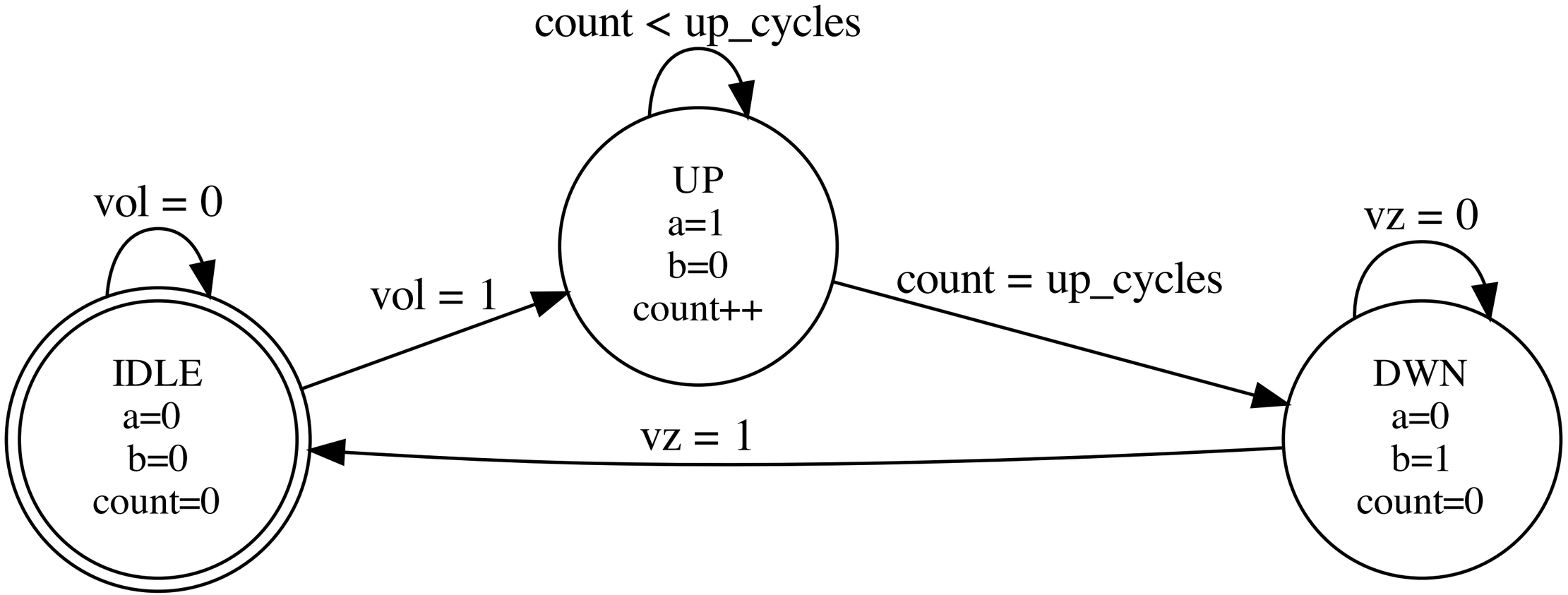

0.6
0.4
0.2
0.0
Ix
Io
1.00
0.75
0.50
0.25
0.00
vo
1
0
A
0
2
4
6
8
10
Time [us]


0.06
0.04
0.02
0.00
−0.02
−0.04
−0.06
Ix
Io
0.990
0.989
0.988
0.987
vo
1
0
A
13.60
13.65
13.70
13.75
13.80
13.85
13.90
13.95
14.00
Time [us]

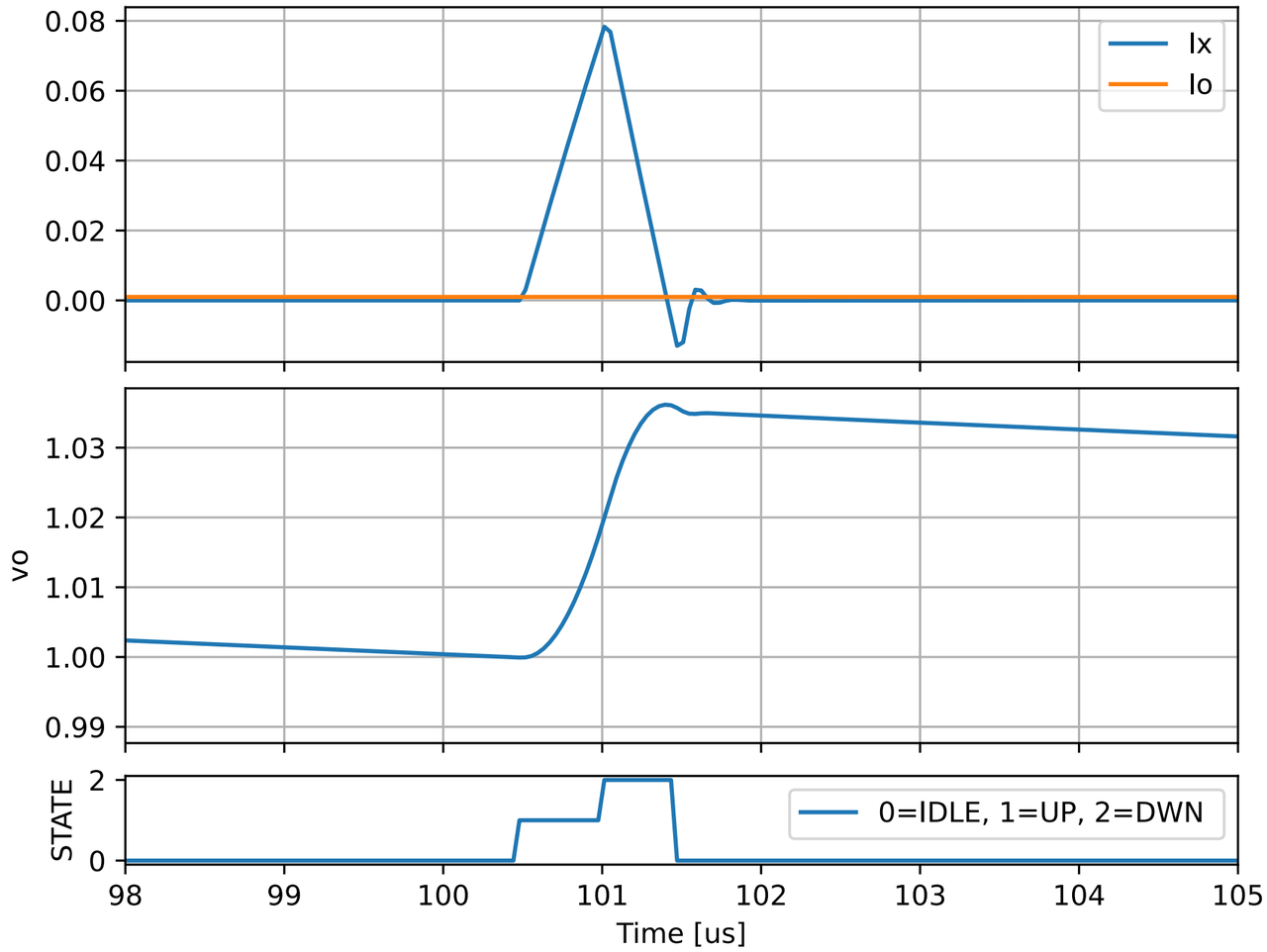

U1A
nRF5340
VDD_nRF
VDD_HV
A19
A21
A27
G31
B8
B10
A15
L1
J1
E1
L2
10µH
L3
10µH
L4
10µH
C2
1.0µF
C3
1.0µF
C4
2.2nF
C16
1.0µF
C5
1.0µF
C19
2.2µF
C20
4.7µF
1
2
3
VDD
DCC
DECR
DECRF
DCCD
DECD
DCCH
VDDH
B28
E31
N31
AL25
AL11
AL7
AG1
U1
C1
AJ31
AL17
AL3
AC1
C8
100nF
C9
100nF
C10
100nF
C11
100nF
C12
100nF
C13
100nF
C14
100nF
C15
100nF
XC2
XC1
B30
C31
X1
32MHz
ANT
L31
L1
2.2nH
C1
0.7pF
RF
C21
N.C.
RESET
SWDCLK
SWDIO
AC31
W31
AA31
D-
D+
B4
B2
D N
D P
VSS
A25
B12
B26



Pulsed Frequency Mode (PFM)


count < up_cycles
UP
a=1
b=0
count++
vol = 0
vol = 1
IDLE
a=0
b=0
count=0
count = up_cycles
vz = 0
DWN
a=0
b=1
count=0
vz = 1

Jupyter PFM BUCK model



Thanks!